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MODEL 1650-D
LOGIC ANALYZER

PRELIMINARY

OPERATING AND SERVICE MANUAL

biomation

10411 bubb road, cupertino, california 95014 (408) 255-9500 twx 910 3380 226

IMPORTANT NOTE

This preliminary manual is supplied to permit earliest possible delivery of instruments. Additional and more complete information will be included in a subsequent final edition of this manual.

Under normal circumstances, all owners of the Model 1650-D Logic Analyzer who receive this preliminary manual with their unit will automatically receive a copy of the final edition.

IF FOR SOME REASON A FINAL EDITION IS NOT RECEIVED, PLEASE CONTACT THE BIOMATION FACTORY, GIVE THE SERIAL NUMBER OF THE UNIT AND COMPLETE RETURN ADDRESS INFORMATION.

OPERATING AND SERVICE MANUAL

MODEL 1650-D

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SECTION I

GENERAL INFORMATION

1.1 Certification

Biomation Corporation certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages.

1.3 Instrument Description

The 1650-D Logic Analyzer is a new instrumentation tool for the design and repair of digital logic circuits. Complex logic timing relationships can be conveniently recorded, displayed and analyzed. Sixteen channels of digital information can be recorded and monitored at rates up to 50 MHz.

The Biomation Model 1650-D is designed specifically for analysis of digital logic circuits and signals. The unit can be used on both synchronous and asynchronous signals and can detect random logic pulses as narrow as 5 nsec (250 mV overdrive typical) with the use of the "LATCH" input feature.

The Model 1650-D Logic Analyzer provides the ability to measure up to sixteen digital signals against a preset threshold, update the detectors with an internal or external clock, and store 512 such simultaneous decisions for each input signal. Threshold settings are independently selectable for Channels 1-8 and 9-16. This information is then presented for display on an oscilloscope in a sixteen trace timing-diagram presentation. Thus, the user can capture unique combinations of digital events for concise and rapid analysis.

The Model 1650-D is a bench-type instrument with tilt-up stand and may be rack mounted as a single unit with the factory option rack mount kit, which occupies a 6.25-inch vertical space in a standard 19" wide rack.

Specifications for the Model 1650-D are given in the following paragraphs.

1.4 Specifications

SIGNAL INPUTS

Number. 16.

Impedance. 1 MΩ/10 pF. Inputs greater than ±12 V clamped to ±12 V through 10 kΩ.

Two Threshold Controls. Channels 1-8 independent from Channels 9-16. Selectable TTL, ECL, MST, +2.5, -2.5, and +2.0. Continuously variable ±2.4 V. Selectable for X1 or X10 probes.

Max Input Voltage. ±50 V continuous, ±100 V transient.

Input Modes. Selectable; SAMPLE or LATCH.

Sample Mode. Unit stores the detected logic level present at each active clock transition simultaneously on all input channels. Maximum channel-to-channel time skew of this clocked data <1 nsec. Minimum pulse width always detected and recorded is one clock plus 2 nsec with 250 mV or more threshold voltage overdrive.

Latch Mode. Threshold detector latches in state opposite that stored at previous clock transition in the event that multiple transitions of the threshold occur prior to the next clock transition.

Minimum Pulse Width to Latch. 5 nsec with typically 250 mV overdrive beyond actual threshold.

CLOCK

Internal. Selectable 0.02, 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, microseconds or milliseconds clock intervals.

External. Via front panel BNC connector, continuous rates from 50 MHz to DC. External clock signal threshold set on threshold selection

for Channels 9-16. Positive or Negative edge may be selected. 1 MΩ input. Fixed delay between input data signals and external clock input at the threshold detectors is typically 13 nsec.

TRIGGER

Source. Selectable; internal, external or manual.

Internal. Combinational triggering; Selectable "1, Don't Care or 0" for all 16 channels. May be triggered when selected combination appears at inputs or triggered when combination disappears from the 16 inputs.

External. Via rear panel BNC connector, ECL level or I/O connector, TTL level.

Static Delay. With Delayed Record Mode selected and the settable Trigger Delay at zero, the fixed delay between the detected trigger and the first stored data in the memory is 4 sample intervals.

Jitter. Data from repetitive record cycles with respect to the input signals will exhibit ± 1 clock interval maximum time jitter.

MEMORY

Size. 16 X 512 bits.

Record Mode. Selectable Pretrigger and Delayed record modes.

Pretrigger. Start via front panel momentary ARM switch, auto start selection or via rear panel BNC, ECL level or via TTL level into I/O connector (0-500 pretrigger samples). Stop via trigger detection and after selectable delay, or via front panel momentary switch.

Delayed. Selectable trigger delay via front panel decade switches to 9999 clock periods, in single clock increments. Record starts after trigger delay has elapsed and stops when 512 bits per channel have been recorded.

DISPLAY OUTPUTS

X Output. Repetitive 1 V p-p ramp waveform 0.5-msec period.

Y Output. Repetitive 1-msec stair step ramp, each step equally spaced in amplitude. Data for each

channel modulates each respective step level. Full range nominally 0 to +1 V.

Z Output. Nominal zero to +5 V pulse. 0.5 msec wide synchronized with X ramp.

$\overline{Z}$ Output. Nominal +5 V to zero pulse. 0.5 msec wide synchronized with X ramp.

Cursor. Movable display cursor.

Expansion. X5, X10, X20 full expansion or mixed expansion. Mixed expansion X1 to left of movable cursor and X5, X10, or X20 expand to right of cursor.

Display Channels. Display output selection for each channel. ON or OFF switches provide the flexibility of viewing 1 to 16 channels. Automatic vertical expansion X1, X2, or X4 dependent on number of channels selected.

DIGITAL INTERFACE

Data. Output, 8 bits parallel, TTL levels positive true, byte serial asynchronous data transfer under control of Flag and Command signals. Channels 1-8 loaded on first command, Channels 9-16 on second command. Rates 120 K bytes down to DC.

Flag. Output of positive TTL transition indicates data word on output lines can be read. Minimum pulse width of 1 μsec.

Command. Input of negative TTL transition requests next data word. Minimum pulse 2 μsec.

Output Request. Input of TTL low or ground stops the display and initiates the digital data output.

Internal Clock Output. Used for connecting several 1650-D units together for synchronous recording, ECL level.

Internal Trigger Input/Output. Used for connecting several 1650-D units together for simultaneous triggering, ECL level.

Internal Arm Input/Output. Used for connecting several 1650-D units together for synchronous arming, ECL level.

MISCELLANEOUS

Operating Temperature Range: 0-50°C.

Power: 100 V/120 V/220 V/240 V RMS, 50-60 Hz.

Size: Height: 6.25 in. (15.9 cm). Width: 17.0 in. (43 cm). Depth: 19.0 in. (48.3 cm).

Weight: Approximately 35 lbs. (18.2 kg).

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model 1650-D.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or Biomation in Cupertino, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

Line Voltage: The Model 1650-D may be operated from either 110 V/120 V/220 V/240 V power lines. A rear panel line voltage switch permits quick and safe conversion for operation from either voltage.

CAUTION: Before plugging instrument into AC power line be sure line voltage PCB is properly located in fuse compartment.

Power Cable: The Model 1650-D is equipped with a detachable 3-wire power cable. Proceed as follows for installation:

a) Connect line-cord plug (3-socket connector) to AC line jack at rear of instrument.

b) Connect plug (2-blade with round grounding pin) to 3-wire (grounded)

power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only 2-blade outlet is available, use connector adapter, then connect short wire from side of adapter to ground.

2.5 Preparation for Use

The Model 1650-D is not a "self-contained" instrument in that it must be interfaced with other types of instrumentation for the data to be visible or analyzed. The following sections of this manual cover operation, set ups, and interface requirements.

2.6 Initial Warm-Up

Although the Model 1650-D is a solid state instrument, a brief warm-up period of approximately 5 min. is required for the input amplifiers and comparators to reach thermal stabilization. This warm-up period is recommended for both the Model 1650-D and its associated output device.

SECTION III

PRINCIPLE OF OPERATION

3.1 Basic Functional Description

The Model 1650-D offers convenient and useful capabilities for the analysis of digital signals. The unit is a sixteen-channel solid-state digital recorder, which operates at a maximum record rate of 50 MHz simultaneously for all sixteen channels. Figure 3.1 presents a block diagram of the 1650-D.

The memory in the 1650-D stores a 512-bit record for each of the sixteen channels. This memory "snapshot" may be taken in either of the following record modes: Pretrigger or Delayed mode. In the Pretrigger mode the recording process begins upon activation of ARM switch or Remote Arm input. The unit continuously monitors and records the status of the sixteen input lines at the selected clock rate. When a trigger event occurs, recording is terminated (or continued until the selected trigger delay has elapsed). Selection of the delay determines the position of the "snapshot" before and after the trigger event. In the Delayed mode the recording process begins at the (delayed) trigger event. This means that the "snapshot" may be delayed downstream from the trigger event at a selectable number of sample intervals (0 to 9999). Therefore, sixteen points in a digital circuit can be continuously monitored, waiting for a specific fault or logic event. When the event occurs, a contiguous record of events before and after (Pretrigger mode) or a delayed recording (Delayed mode) is made for display and subsequent analysis.

3.1.1 Input Threshold

The definition of a stored data signal as a binary "1" or "0" is determined by switch-selected logic threshold levels. Channels 1-8 are independently selectable from Channels 9-16. Six standard threshold levels are available on each of these two switches as well as independent, contiguously variable controls. Standard threshold selections are TTL, ECL, MST, +2.0, +2.5 and -2.5. The VAR position controls provide +2.4 V continuously variable for both the input threshold level selections. In addition, selection of X1 or X10 probe input selection provides full threshold sensitivity for X10 attenuated, higher bandwidth probes.

3.1.2 Sample Mode

In the "SAMPLE" mode of operation, the input levels are strobed into the memory as "1" or "0" based on the signal level with respect to the selected threshold at the time of the active edge of the clock.

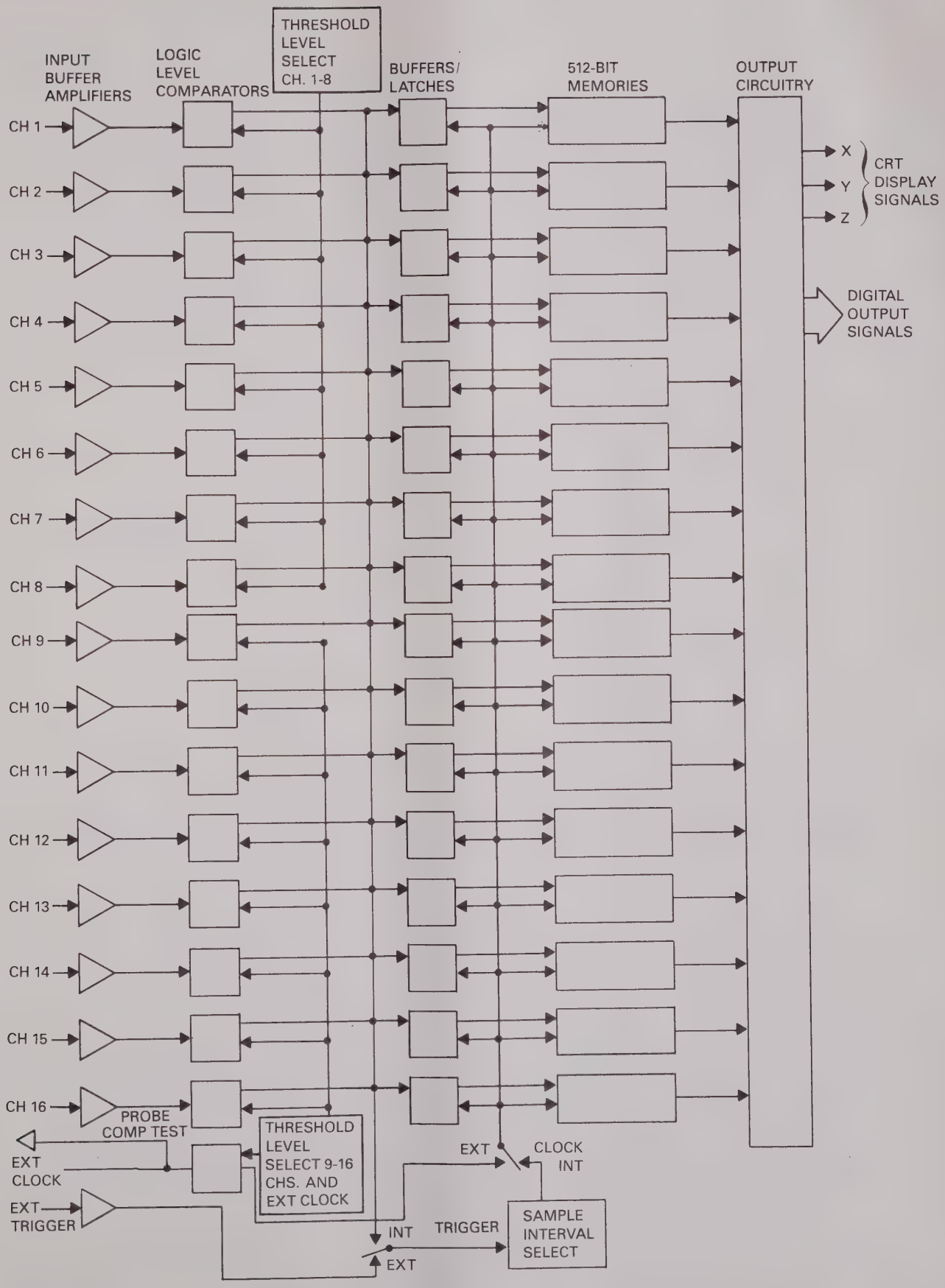

Figure 3.1 Block Diagram of 1650-D

3.1.3 Latch Mode

The "LATCH" mode of recording permits narrow spikes to be recorded. Any spike (positive or negative) with sufficient amplitude and duration causes an input latch to set. This changes the state of the next bit to be written in memory. In this way, narrow spikes or "glitches" occurring at random times between sample clock transitions can be captured.

Typically, a glitch that exceeds the threshold by 250 mV threshold overdrive can be as short as 5 nsec and still be detected. See Figure 3.2.

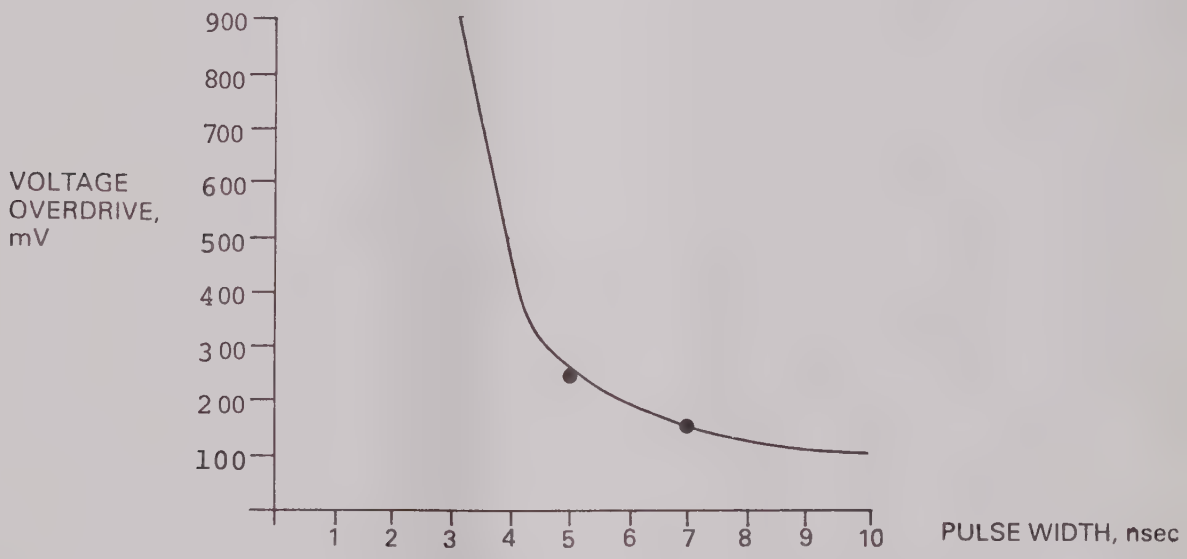

Figure 3.2. Relationship between voltage over threshold and pulse width of glitch that can be typically latched in the LATCH mode of operation.

3.1.4 Signal Inputs

The sixteen signal inputs and the clock input all have an input impedance of 1 MΩ, 10 pF.

3.1.5 Record Rates

The internal clock interval is switch selectable from 20 msec to 0.02 μsec, in a 1-2-5 sequence. The clock of the device or system under test may be input via the front panel to effect synchronous recording, a distinct advantage when synchronous logic is being examined. The external clock logic threshold is set by the Channel 9-16 threshold selector switch. Falling or rising clocking edge is also selectable.

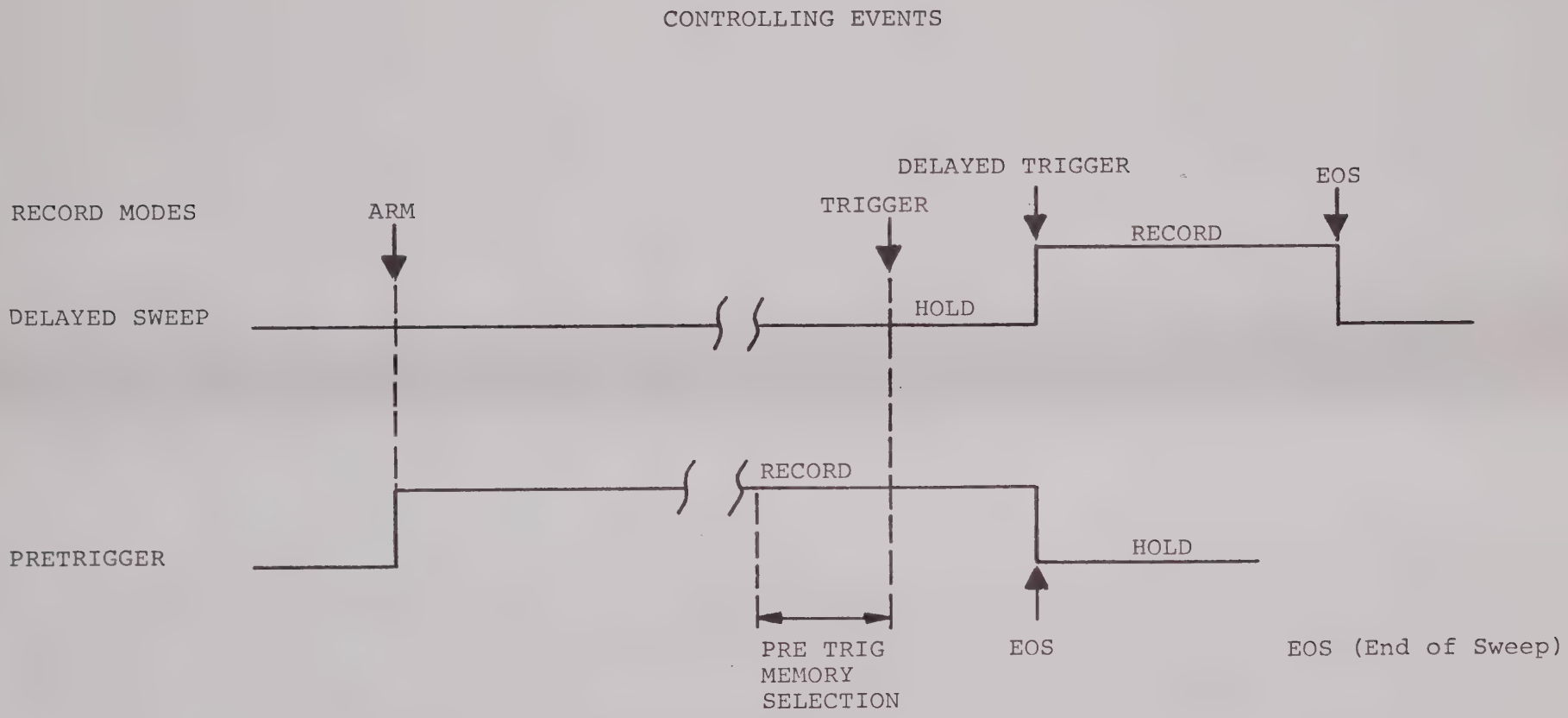

Figure 3.3 Model 1650-D Recording Control Functions

In the Delayed mode a static delay of 4 sample intervals exists from the trigger event until data is stored in the memory of the 1650-D. The Pretrigger mode must be used to observe the trigger event and the three samples directly following that event.

3.1.6 Delayed Record Mode

A Delayed record sequence is started by the Trigger function and stops after the entire memory has been refreshed. The trigger function can be derived from a parallel combination of input signals, true or false from an external source, or manually. The trigger can also be delayed by as much as 9,999 clock intervals in single clock increments. This mode and the Pretrigger record mode are illustrated in Figure 3.2.

3.1.7 Pretrigger Record Mode

The Pretrigger record mode is unique and very useful. With the Pretrigger mode selected, the unit begins recording upon receipt of the Arm command, and continuously updates the memory with new data (destroying the "oldest" data) much like recording with a tape loop. The amount of trigger delay selected determines the amount of prior-trigger data stored when recording ceases; e.g., selection of a 250 clock interval trigger delay will cause the unit to continue recording for 262 clocks after the trigger, and then cease recording, while retaining 250 words of contiguous prior trigger data. In this way, sixteen points in a digital circuit can be continuously monitored, waiting for a specific fault or logic event to trigger the unit. When the trigger occurs and the delay is counted out, a contiguous record of events (before and after the trigger) is recorded and displayed.

3.2 Recording Considerations

Because the Model 1650-D can record as a function of either the internal clock or an external clock, note should be taken of some basic differences in these two methods.

When the internal clock is used for recording, no particular phase relationship will exist between this clock and any synchronous information rate in the signals being recorded. Therefore, a beat frequency can exist between these two basic rates. If the 1650-D internal clock is at least 10 times higher in frequency than the signal rate, very little effect will be noted in the recorded data. For high signal rates (with respect to the record clock), a beat rate effect can be seen by varying widths in the recorded "pulses" and even periodic "dropped" bits will be observed when these rates approach the limiting ratio of two to one.

When the synchronous clock used for the generation of the input signals to the 1650-D is used as the record clock in the 1650-D, no phase errors exist and no beat frequencies will be evident; i.e., the beat note is zero frequency. In this case, signals with information rates up to and including 1/2 the clock frequency can be recorded, without distortion. This is called synchronous recording. The fixed delay between input data signals and the external clock input at the threshold detectors is typically 13 nsec. See Figure 3.4.

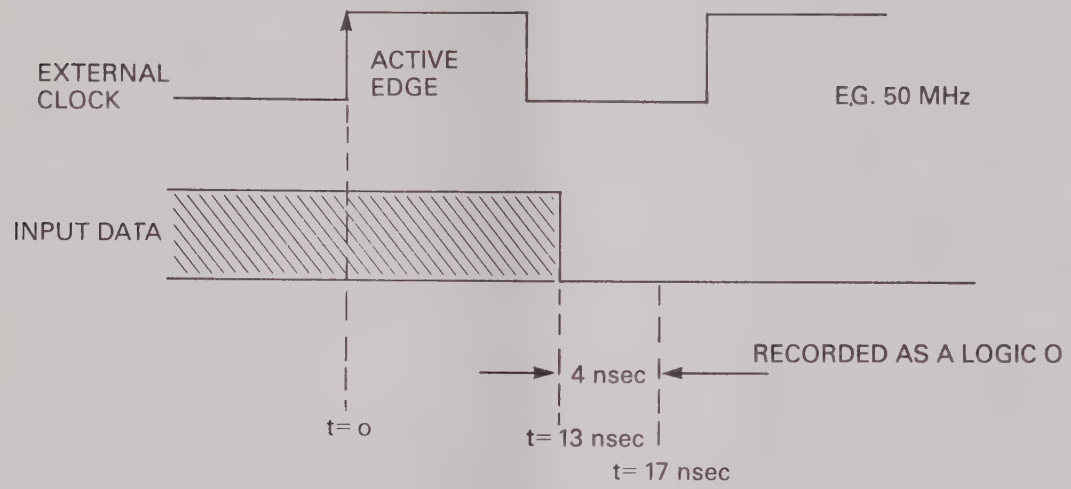

Figure 3.4. Sample mode timing requirement. When using an external clock, data may change states anytime up to typically 13 nsec after the active edge of the clock. Once the logic state change is made, it must be maintained until 17 nsec after the active clock edge to be recorded in that state.

Bear in mind that the 1650-D is an instrument for the detection and storage of digital data. As such, the unit only discriminates between two different levels as defined by the threshold switches. The data stored and displayed is NOT an analog representation of the input signals, but a pattern of "ones" and "zeros" that represent threshold crossings.

3.3 Outputs and Control Inputs

3.3.1 Display Output

Once Record is terminated, the unit automatically goes into a display mode where the contents are repetitively output to a CRT or triggered scope.

The display presentation can be formated with the Model 1650-D front panel controls. The user may select to display from 1 up to all 16 channels of recorded logic. The logic

channels are displayed in successive order with Channel 1 at the top of the display sequence. Further, the Model 1650-D automatically provides vertical expansion of X2 and X4 for selections of 8 to 5 channels and 4 to 1 respectively. This means that 9 to 16 channels will occupy 1/2 vertical division of the display per line, 5 to 8 channels selected will occupy 1 division per line, and 1 to 4 channels selected will occupy 2 divisions per logic line. This assumes 0.1 V/division vertical display calibration.

With no horizontal expansion, 500 bits of information per line are displayed, 50 per division. The 1650-D has a movable display cursor. This cursor may be used to chose the point of display expansion. Display expansion may be selected in a mixed mode or in full expansion. In the mixed expansion setting, the display appears as X1 expansion to the left of the movable cursor and X5, X10, or X20 selectable to the right of the cursor. Full expansion provides 100 bits per line in X5, 50 bits per line in X10, and 25 bits per line in X20 expansion.

3.3.2 Digital I/O

The digital data in the Model 1650-D's memory can be output under the direction of two digital control inputs via the rear panel, 24-pin digital interface connector. These inputs are the OUTPUT REQUEST line and the COMMAND line. Once digital output has been requested the 1650-D loads an 8-bit parallel word on the output buffers, signaling the receiving device with a FLAG output signal. These 8 bits are the Channel 1-8 samples. The second command input gates are Channels 9-16. Successive bytes may be strobed onto the output buffers by the COMMAND input up to a maximum strobe rate of 120 K bytes per second. All data outputs are in TTL levels, positive true. Other input control lines, as well as output status signals, are available at this connector. See Section V for complete details.

3.4 Operational Functions

The operation of the Model 1650-D is basically concerned with the signals or events that determine the initiation and termination of the sampling and recording of the input signals and events, and their interrelationships in the functional operation of the unit.

3.4.1 Sweep and Sweep Time

In the following discussions the terms "sweep" and "sweep time" are often used. The term "sweep" is used to designate the succession of samples taken on the input signals during a recording sequence. The term "sweep time" is used to designate the amount of time required to fill the

memory with contiguous samples of the input signal. When this term is used, it is normally assumed that the entire sweep was accomplished at a single linear sample rate.

3.4.2 Arm, Trigger, and End of Sweep Function

The Arm, Trigger, and End of Sweep (EOS) functions, together with adjustable delay (associated with the Trigger event), control the sequence of events in the operation of the record cycle of the Model 1650-D. The effect of each of these functions or events on the sequence of events is dependent upon the mode of operation selected for the unit. This interdependence will be described below.

In all recording modes, an Arm function must precede a Trigger function. The unit cannot be triggered before it is armed. The Arm function may be initiated manually via front panel pushbutton or externally via rear panel input. Once the unit has been armed, it can accept a trigger.

The Trigger function may also be initiated in the same manner as the Arm function. In addition, the unit may detect a Trigger from any one channel, or via the coincidence of a parallel combination of bits as selected on the front panel. Furthermore, the combinational trigger selection allows the 1650-D to trigger when the selected parallel combination becomes true on the inputs or, when it no longer coincides with the selections, becomes false.

3.4.3 Modes of Operation

The operational modes for the record sequence in the Model 1650-D are determined by the record mode selected. Three record modes are provided. They are Pretrigger, Delayed Manual, and Delayed Auto. The Delayed modes are identical in operation except for derivation of the Arm signal. In the Delayed Auto mode the Arm signal occurs automatically after a record sweep and one complete display output sweep. In the Delayed Manual the Arm signal must be provided by activation of the front panel switch or an external signal input to the rear panel. For purposes of further discussion, Delayed Auto and Delayed Manual will be treated as Delayed Record Mode. See Figure 3.3 for an illustrative reference.

3.4.3.1 Delayed Record Mode

In the Delayed record mode, the record cycle is initiated by the (delayed) Trigger, and is ended at the End of Sweep (EOS), at which time all 512 bits/channel of the memory have been loaded with new data. In the Delayed mode, there exists a four-sample delay between the start of the record cycle and storage of data in the memory. This means that the 512 word "snapshot" is taken four clocks downstream

from the (delayed) triggering event. This mode can be used in various ways depending on the setting of the Trigger delay. With the delay set to zero, recording begins at the trigger event and ends 516 clock intervals later. With a delay set into the Trigger delay selector, recording is held off until after receipt of the trigger and timing out of the trigger delay. When the delay has elapsed the recording process begins, ending again after 516 clock cycles.

The delayed sweep mode of operation is used in situations where the only good trigger signal precedes the data to be recorded. In many cases the delay between the Trigger and the desired information is greater than the optimum sweep time. In these cases the signal would not be recorded with sufficient resolution to be useful. By delaying the initiation of the sweep with the Trigger delay and sampling the signal at a faster rate, the information can be recorded with good time resolution.

3.4.3.2 Pretrigger Mode

Pretrigger recording is a unique feature of Biomation Recorders. Pretrigger recording allows the capture or recording of signals that are not known to be significant for recording until after the signal has occurred. Another good use of this mode is in cases where the only good Trigger available follows the information of interest.

In the Delayed record mode the starting point for filling the memory with new information is when the Trigger occurs, or later. In the Pretrigger record mode of operation the memory is continuously being updated after the unit has been Armed, and will discard information (from the "other end" of the memory) at the same rate. When a trigger event occurs, the 1650-D saves the selected Pretrigger portion of memory and continues recording until the remaining portion is filled with data occurring after the trigger event. If the PRE-TRIG memory switches have been set to 100 bits, the memory will contain 16 X 100 bits of pretrigger and 16 X 412 bits of data recorded after the trigger.

3.4.3.3 Delayed Auto Mode

The Delayed Auto Mode allows the Model 1650-D to ARM itself after a single display sweep. This provides a continuously updating display upon recognition of each defined trigger event.

SECTION IV

OPERATION

4.1 Introduction

This section identifies and describes front panel controls, rear panel connections, and typical operating procedures. Included are complete descriptions of front panel controls and their effective ranges, location and proper use of rear panel connectors, set up procedures prior to using the Model 1650-D, and step-by-step operating procedures for various modes of operation. A thorough understanding of this section is essential to the successful use of the instrument.

4.2 Front Panel Controls and Connectors

4.2.1 Control Clusters

The controls of the Model 1650-D may be divided into five groups. Each group contains separate controls with related functions. Figure 4.1 is a front panel photograph of the 1650-D. The five control groups are as follows:

Record Mode and Trigger

Input Mode and Thresholds

Clock

Display

General

4.2.2 Record Mode and Trigger

(1) RECORD MODE. In the PRE-TRIG position, the unit fills the memory with new data when the front panel MANUAL ARM switch or remote Arm inputs on the rear panel are activated. Recording continues, dumping the oldest data off the end of the memory until the trigger event occurs. At that time the portion of the memory selected (PRE-TRIG MEMORY (2)) is saved. The reamining portion of the memory is filled with new data contiguous to the trigger event.

In the DELAY MAN mode, an Arm initialization alerts the 1650-D that it may accept the next designated trigger event. When that event occurs, the TRIG DELAY starts. When the selected trigger delay has elapsed (0 to 9999 clock intervals), the memory begins to fill with new data continuing until 512 bits/channel have been recorded.

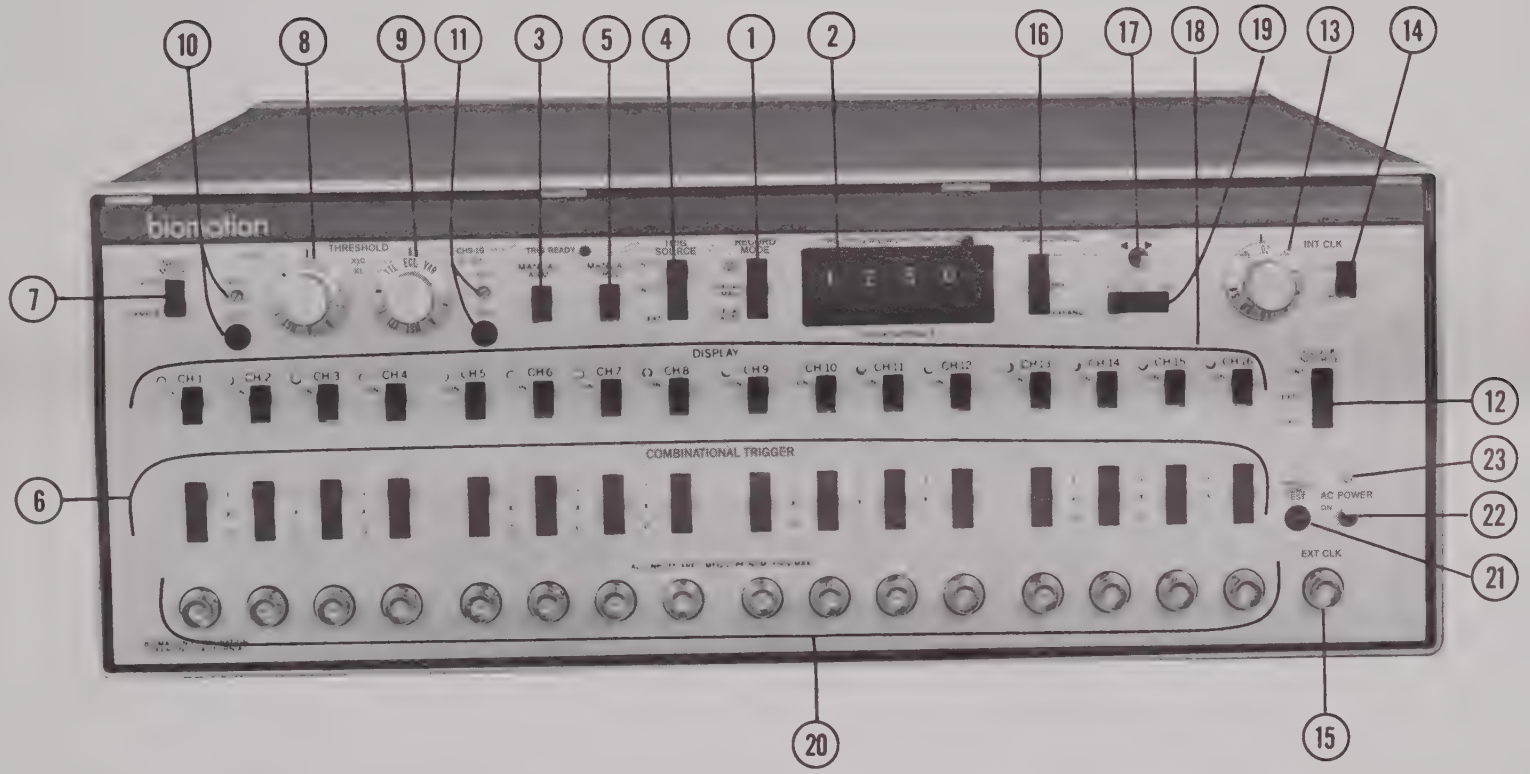

Figure 4.1 1650-D Front Panel

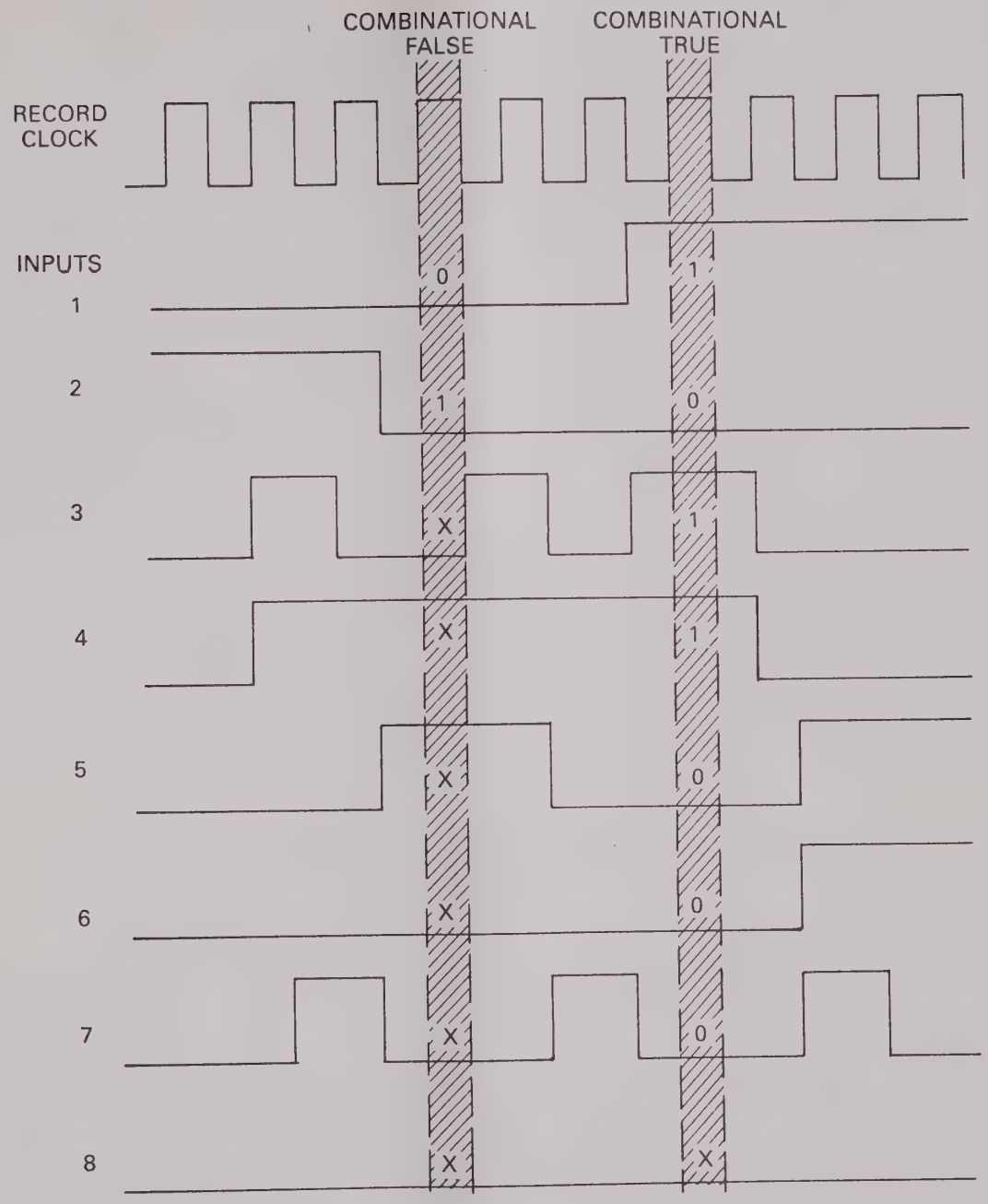

Figure 4.2. This diagram illustrates an example of conditions for combinational true and combinational false triggering. Notice that the CMBL (F) trigger condition occurs during the clock cycle for which the combination of inputs no longer coincides with the trigger combinations selected.

In the DELAY AUTO mode, the Arm function is activated by the 1650-D internally. Recording is accomplished exactly as is done in the DELAY MAN mode. Once the 1650-D has completed a single display output sweep (requiring 16 msec), the unit automatically re-arms itself and will accept the next designated trigger event. This mode of recording is very convenient for initial set-up because no manual or external Arm input signal is required for acceptance of a trigger event.

(2) PRE TRIG MEMORY/TRIG DELAY. In the PRE TRIG RECORD MODE (1), these convenient digitswitches allocate the portion of the Model 1650-D's memory that is saved for prior trigger information. Note that the memory displayed is 500 bits/channel long. Setting these switches to 500, therefore, will place the trigger event at the end of the display memory. The 499 bits/channel displayed to the left of this trigger location were recorded prior to the trigger, thereby giving a look back in time from a trigger event. Attention should be paid to the amount of time between initialization of the Arm function and recognition of the Trigger event. If after arming the 1650-D only a 100-clock interval period elapsed before the trigger event was recognized with the PRE TRIG MEMORY selection set to 500, the unit would not have had sufficient time to record all 500 pretrigger samples. Therefore, 400 samples/channel would be left in the memory from a previous recording.

CAUTION: Setting the PRE-TRIG memory to greater than 500 samples is an illegal mode for the Model 1650-D.

The memory is 512 bits/channel long. The first 500 bits/channel are specified to be valid data samples. The display output sweep consists of only these 500 bits/channel.

In the DELAY MAN or DELAY AUTO modes, the PRE TRIG MEMORY/TRIG DELAY designates the amount of delay that elapses prior to the record start. When a trigger event is recognized by the Model 1650-D, the beginning of the record cycle may be postponed from 0 to 9999 clock intervals. The inherent static delay causes the stored data to lag this delay setting by 4 sample intervals.

(3) MANUAL ARM. Pressing this momentary switch starts the unit recording when the RECORD MODE switch (1) is set to PRE TRIG. In DELAY MAN mode it alerts the 1650-D to accept the next trigger event. When recording in the pretrigger mode, the entire memory may be set to all "zeros" (low) by holding the Arm switch down for a minimum of one single sweep (500 X sample interval).

(4) TRIG SOURCE. Selects origin of the trigger event. INT(T) causes the unit to continuously monitor the 16 input signals upon activation of the Arm function when the inputs coincide (become true) with the COMBINATIONAL TRIGGER (6) selection, a trigger pulse is generated. See Figure 4.2.

In the INT(F) source, the 1650-D observes the input channels waiting until the input combination no longer coincides with the trigger selection. In other words, the input signal combination becomes "false" with respect to the trigger combination switches.

In the EXT source, the unit looks for a trigger pulse (ECL level or TTL level) from the rear panel BNC TRIG IN or I/O connector, respectively.

(5) MANUAL TRIG. Pressing the Manual trigger momentary switch provides an overriding trigger pulse into the 1650-D in any TRIG SOURCE (4) selection. The unit will only recognize this trigger, of course, once the Arm is activated.

(6) COMBINATIONAL TRIGGER. These switches may be used to select any one or a combination of channels as a trigger source. The 16 switches have three positions: "1" (high), "X" (Don't Care), and "0" (low).

4.2.3 Input Mode and Thresholds

(7) SAMPLE/LATCH. In SAMPLE position, the unit compares input levels with the preselected threshold level and stores a high or low, as appropriate, on the positive transition of the clock. Thus, the data stored in memory reflects the input states at the clock transition.

In the LATCH mode, the unit stores as above for single threshold transitions in a clock period, but also "latches" to a state opposite that last stored when multiple transitions occur in a clock period. For instance, a single narrow pulse between clock transition would not affect the memory contents in SAMPLE mode but would affect the stored data in LATCH mode. This "glitch" catching feature works for either positive or negative pulses by "stretching" the random pulse to one full data period. The 1650-D will typically "latch" on pulses as narrow as 5 nsec. See Figure 4.3.

(8), (9) THRESHOLD, VOLTS. Provides switch selection of MST (0.0 V), TTL (1.4 V), ECL (-1.3 V), A (+2.5 V), B (-2.5 V), C (+2.0 V) thresholds, as well as (VAR). The A, B, and C threshold levels are individually variable between $\pm$5 V. Adjustments are internal to the instrument and are clearly labeled on the front panel PC board. These

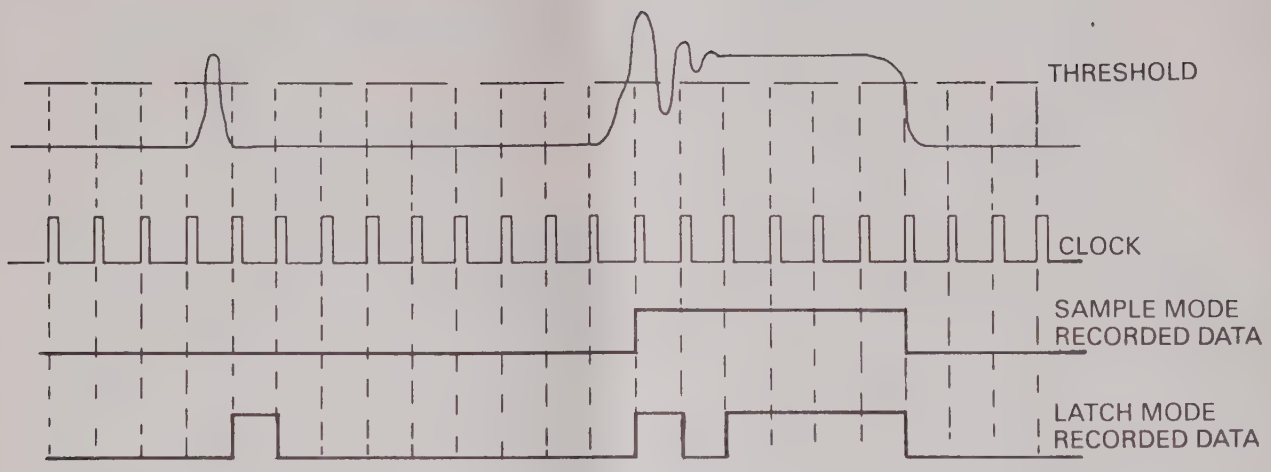

Figure 4.3. This diagram illustrates two ways in which the LATCH mode of recording can provide valuable information about the circuit signal that cannot be positively captured with the SAMPLE mode of recording.

two switches are set independently for Channels 1-8 and 9-16. The black nomenclature is for use with unattenuated (X1) probes; red nomenclature is for use with X10 attenuated probes. In the VAR position, the user may adjust the vernier threshold settings using the potentiometer marked CH 1-8 ADJ for Channels 1 through 8, and the potentiometer marked CH 9-16 ADJ for Channels 9 through 16. A test point is provided to the right of each potentiometer for observation of each setting.

When the input level is more positive than the threshold, a logic "one" (high) is stored in memory; when the input is less positive, a logic "zero" (low) is stored.

(10), (11) VARIABLE TEST. To set a vernier threshold, set THRESHOLD (CH 1-8 and/or CH 9-16) to VAR. Adjust CH 1-8 and/or CH 9-16 potentiometer with a screwdriver for the desired threshold as measured at the test points, adjustable $\pm$2.4 V. The output impedance at this test point is 10 kΩ. The accuracy of the threshold voltages are nominally $\pm$5% of maximum threshold readings.

4.2.4 Clock

(12) CLOCK SOURCE. Selects internal (INT), external rising edge (EXT ∫), or external falling edge (EXT ∖) clock source. With (INT) selected, the INT CLK (13) switch is used to provide the sample rate for strobing the input data signals. (EXT ∫) or (EXT ∖) activates the EXT CLK BNC connector (15). The unit will not record until an external clocking signal is provided.

(13) INT CLK. Selects, in conjunction with the µsec/msec switch (14), the choice of internal clock intervals of 0.02, 0.05, 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, 10.0 and 20.0 µsec/msec clock input.

(14) µSEC/mSEC. Provides multiplication factor for switch (13).

(15) EXT CLK. This BNC connector allows input of an external clock when switch (12) is either in the EXT ∫ or EXT ⌇ position. Input impedance 1 MΩ. Clock threshold set by CH 9-16 voltage threshold switch (9).

4.2.5 Display

(16) DISPLAY. The display defines the horizontal expansion mode to be used. The (X1) position display output consists of the 16-line timing diagram of 500 bits per line. A more detailed view of any portion of this display may be obtained by moving the vertical line cursor to the point of interest using the EXPAND POSITION (17) control, selecting (MIXED) or (EXPAND) positions.

The (MIXED) position provides X1 horizontal expansion to the left of the movable cursor and X5, X10, or X20 horizontal expansion, as selected on the HORZ switch (18), to the right of the cursor. This mixed mode of expansion allows the user to view data leading up to the point of interest as well as detailed expansion of data to the right of that point.

The (EXPAND) position horizontally expands the timing diagram to X5, X10, or X20 as selected on the HORZ switch (18). The segment viewed on the display begins from the vertical cursor location and contains 100, 50, or 25 bits per line, respectively, with the expansion factor selected. Movement of the EXPAND POSITION control (17) selects the memory location from which the expansion begins.

(17) EXPAND POSITION. This control, when used in conjunction with the DISPLAY switch (16), determines the point of horizontal display expansion. With the DISPLAY switch set in the (X1) position, the expansion control is used to locate the vertical cursor on the time diagram display. The control has two speeds, as well as left and right direction control. Movement of the control stick to the right or left produces a corresponding one-bit horizontal movement of the display cursor. If the control stick is held over for one second, then the cursor will resume movement at a constant rate until the control is released.

The cursor remains visible with DISPLAY (16) set to (MIXED). Data to the left of the cursor remains at X1 expansion while data to the right is expanded to the HORZ (18)

switch selection of X5, X10, or X20. Movement of the EXPAND POSITION control changes the memory location at which this mixed expansion starts.

(18) DISPLAY. These 16 switches provide the user with the ability to select which channels of recorded data are output to the display monitor. The Model 1650-D automatically expands the vertical amplitude of the output waveforms by a factor of 2 and 4, X2 for less than nine channels and X4 for less than five channels selected.

In DISPLAY (16) (EXPAND) position, the display is comprised of 100, 50, or 25 bits/line of data determined by the HORZ switch (19) location. This window of data begins at the signal location where the cursor is positioned. Movement of the EXPAND control slides the cursor, thereby moving the expansion window along the timing diagram.

(19) HORZ. This switch selects the X5, X10, and X20 expansion factor for mixed and full expansion operation of the display output. In full expansion, DISPLAY switch (16) set to (EXPAND), X5 provides a 100 bits/line window of the timing diagram starting at the display cursor location. X10 provides a 50 bits/line window, and X20 provides a 25 bits/line window. At X20, 2.5 bits or samples of the recorded signal per division appear on the CRT or oscilloscope. At the highest recording rate, 50 MHz (20 nsec/sample), the time resolution is 50 nsec/division on the CRT.

4.2.6 General

(20) CH 1 THROUGH CH 16. 16 BNC connectors for input of as many digital signals. Input impedance is 1 MΩ, 10 pF to ground.

(21) PROB COMP TEST. This probe compensation test point is a direct connection to EXT CLK input. Allows user to compensate his probes with respect to the input circuitry of the 1650-D.

The probe to be compensated is connected to EXT CLK, and to a square wave generator. A properly compensated scope probe, connected to an oscilloscope, is placed on the COMP TEST point. The probe at EXT CLK is then adjusted until the square wave on the scope is normal. The 1650-D MUST be powered up to perform this adjustment.

Each of the sixteen probes to be used with the 1650-D may be compensated in this manner. However, each probe must be connected in turn to the EXT CLK input.

(22) AC POWER. When switch is ON, LED (23) lights indicate power has been applied to the 1650-D.

4.3 Rear Panel Connectors (See Figure 4.4)

(1) X Output. Repetitive 1 V p-p ramp waveform, with a period of 0.5 msec. Adjustable 0.7 V to 2.5 V internally.

(2) Y Output. Repetitive 1-msec stair step ramp, each step equally spaced in amplitude. Data for each channel modulates each respective step level. Full range nominally 0 to 0.8 V. Adjustable 0.75 V to 1.25 V internally.

(3), (4) Z and $\overline{Z}$ Output. Z output nominally zero to +5 V pulse, 0.5 msec in duration and synchronized with the X output ramp for CRT retrace blanking. $\overline{Z}$ output inverted pulse of +5 V to zero.

(5) TRIG IN. Used in conjunction with connectors (6), (7), (8), and (9) for synchronization of multiple units for increased input signal capacity. ECL termination. Also used for external trigger input.

(6) TRIG OUT. Output ECL level when the unit recognizes the defined trigger event. Used in conjunction with TRIG IN (5) for synchronization of multiple units for increased input signal capacity. The slaved unit's TRIG SOURCE must be set to EXT.

(7) ARM IN. Input ECL termination for external Arm input or synchronization of multiple units.

(8) ARM OUT. Output ECL level occurring upon activation of the front panel MANUAL ARM switch. Used for synchronization of multiple units.

(9) CLK OUT. Clock output ECL driver. Used for synchronization of multiple units to provide simultaneous recording of all input signals. Must be properly terminated with 50 Ω impedance.

(10) I/O Connector. 24-pin interface connector used for all I/O operations. For procedural detail and pinouts, see Section V. Mating connector Amphenol Micro Ribbon 57-40240.

(11) AC Input, Fuse, Line Voltage Selector. AC input contains a line interference filter. Fuse: use a 1 A Slow Blow for 115 V operation, and a 0.5 A Slow Blow for 230 V operation.

4.4 Set Up Procedure

4.4.1 Initial Set Up

This section describes the connection of a Model 1650-D with a CRT display or oscilloscope and the steps to record and display a known signal.

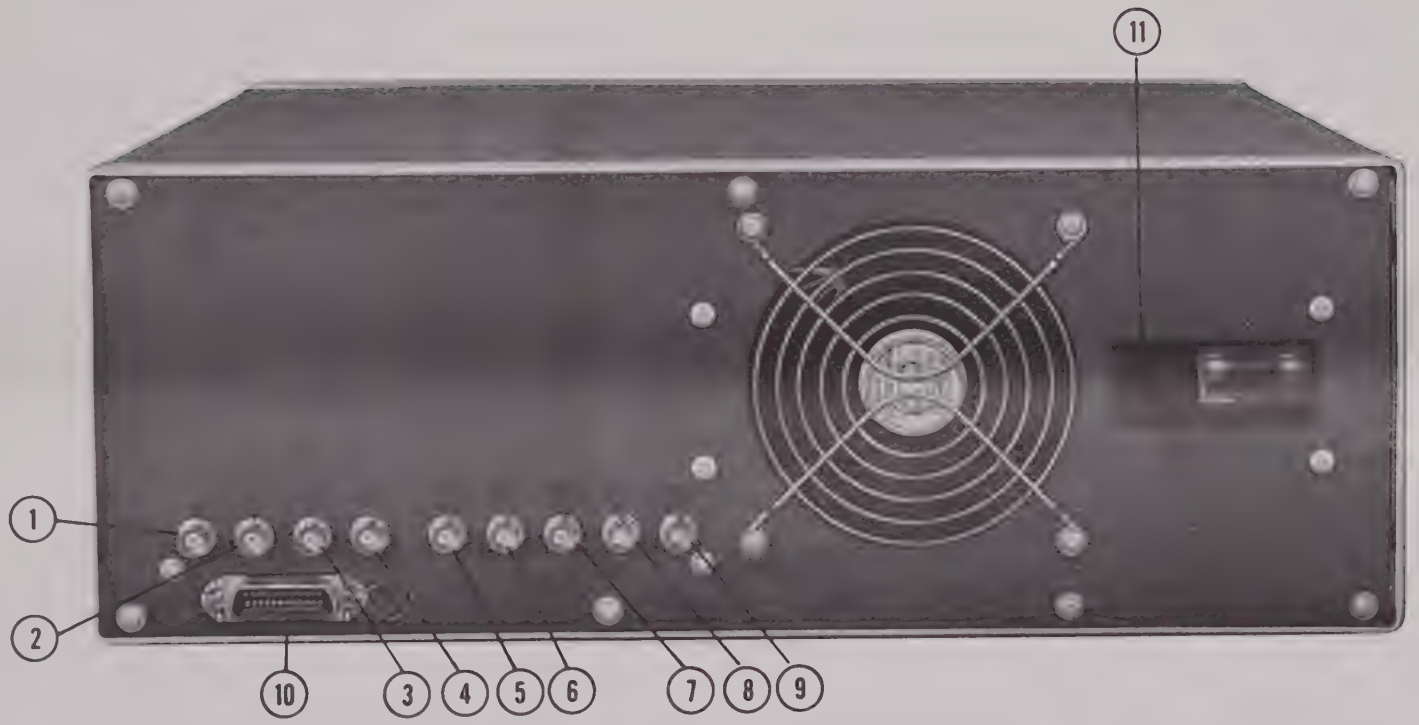

Figure 4.4 1650-D Rear Panel

Before connecting the unit to line power, check the voltage selector PC board in the fuse holder to ensure that it is set to the proper line voltage and be sure that the correct size fuse (as printed on the rear panel) is installed.

Connect the Model 1650-D to a pulse generator with a manual single-pulse capability and CRT display as shown in Figure 4.5a or 4.5b. Depending upon the particular CRT or oscilloscope being used, it may be necessary to use the $\overline{Z}$ output of the 1650-D for the retrace blanking signal.

CAUTION: Some older "tube types" oscilloscopes have a high voltage on the Z axis inputs. THIS COULD DAMAGE THE Z OR $\overline{Z}$ OUTPUT OF THE 1650-D. PLEASE CHECK BEFORE CONNECTING THE UNITS TOGETHER.

Set the units (where appropriate) as follows:

Vertical sensitivity	0.1 V/div. uncalibrated DC coupled
Vertical position	Bottom of display
Horizontal sweep	0.5 msec/div. (Figure 4.5a)
Horizontal sensitivity	0.1 V/div., DC coupled (Figure 4.5b)
Trigger input	-, DC coupled, external (Figure 4.5a)
Pulse Generator	Single manual pulse, 2.5 µsec wide, 0 to +3 V pulses

Set the Model 1650-D as follows:

MODE:	Sample
THRESHOLD:	TTL (1.4 V)
DISPLAY:	X1
INT. CLK:	0.1 µsec
RECORD MODE:	PRE TRIG
TRIGGER:	
PRE TRIG MEMORY:	100
TRIG SOURCE:	Internal
COMBINATIONAL TRIG:	CH 16 "1", all others "X" DON'T CARE

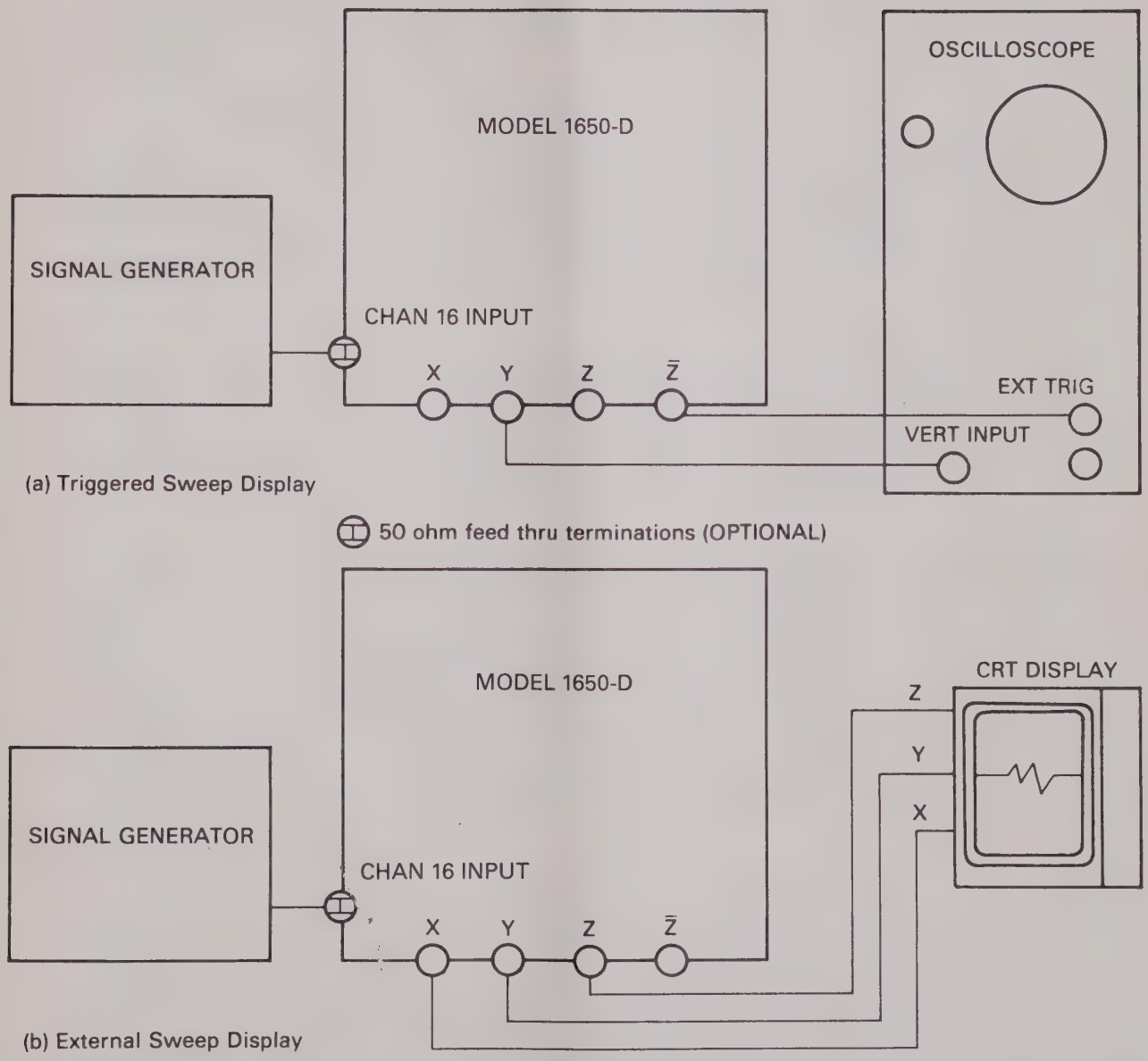

Figure 4.5 Display Interconnections

4.5 Operating Procedures

In this section two modes of operation will be discussed and illustrated. A pulse generator capable of generating a single pulse upon manual command is required.

Set the generator to give single, manually initiated pulses approximately 5.0 μsec wide, and 0 to +3 V amplitude.

4.5.1 Sample Mode

Press MANUAL ARM and pulse the generator. Figure 4.4 illustrates the display obtained. Channels 1 through 15 will display a low level, while Channel 16 displays the pulse. The pulse will occupy one division on the CRT, and be comprised of 50 clock intervals. One hundred clock intervals will have been recorded before the positive transition of the pulse.

4.5.2 Latch Mode

Set INT CLK to 50 μsec. In the SAMPLE MODE press the MANUAL ARM and pulse the generator while watching the display. The 1650-D will trigger only if the leading edge of the internal clock coincides with the high state of the pulse. With a 50 μsec clock and a 5 μsec pulse it can be expected to take as many as 10 repetitions of the pulser for this coincidence to occur.

Now select the LATCH mode. Repeat pressing the MANUAL ARM and pulsing the generator. Observe that the unit captures the pulse each time and represents it with a one clock interval of 50 μsec. This is more readily observable by moving the cursor near the displayed pulse and expanding the time diagram with the HORZ-DISPLAY (EXPAND) switches. This feature is particularly useful for detecting narrow random noise pulses or "glitches". This mode operates in the same manner independent of the chosen clock interval. A glitch typically as short as 5 nsec may be detected and displayed at any clock interval.

4.5.3 Manual Trigger

To verify operation of each channel, change the pulse generator to a repetitive output, approximately 5 kHz rate, with the same pulse as before. Starting with Channel 1, connect the generator to the input BNC. Press the MANUAL ARM switch, and then the TRIGGER MANUAL switch. Several pulses of one clock interval will be displayed on the CRT, on the top trace. Repeat the above procedure for each channel, 1 through 15. The trace corresponding to that channel will display several pulses in turn. The 1650-D should be in the Delayed Record mode with the trigger source set to EXT.

SECTION V

OUTPUT INTERFACE

5.1 Introduction

The output interface of the Model 1650-D includes two methods of analog output: one, using a CRT in an X-Y mode, and two, using an oscilloscope in the triggered mode. These methods are explained in Section 4.4.1.

The instrument also offers a digital output of data. This data is output in an 8-bit parallel format. The bits representing a simultaneous data entry for all channels are presented in two successive 8-bit outputs. Channels 1-8 are loaded on the output buffers to be followed by Channels 9-16 when the first CMD input is recognized. One thousand twenty-four such 8-bit words are available through the digital output mode.

5.2 Digital Output

All inputs and outputs at the 24-pin rear panel connector are positive logic, TTL signals. Direct access to control gates is available at the connector. This connector provides the physical interface for digital data output. The connector is an Amphenol Micro Ribbon 57-30240. The mating connector is an Amphenol part number 57-40240.

The pin assignments and signal descriptions for the digital interface are listed in the following table:

Pin #	Signal Name	Description
18	Data Output 1	These lines supply data stored in memory when the digital output procedure, outlined in Section 5.2.1 or 5.2.2 below, is followed. Buffering is provided.
19	Data Output 2	
16	Data Output 3	
17	Data Output 4	
22	Data Output 5	
23	Data Output 6	
24	Data Output 7	
21	Data Output 8 (OUTPUTS)	
2	Output Request (INPUT)	Line is normally pulled high. To initiate output, pull low to enable TTL level.

Pin #	Signal Name	Description
3	Command (INPUT)	Normally high. Changing to a low level causes unit to "fetch" next data word. The high to low transition time must be 200 nsec or less.
4	Auto Arm Mode (OUTPUT)	0 V when instrument is in Auto Arm, otherwise at -5.2 V (CMOS).
6	1 MHz Clock (OUTPUT)	TTL signal 0.8 μsec high, 0.2 μsec low.
14	Flag (OUTPUT)	Goes high when next data word is available, approximately 100 nsec after command goes low.
7	M>N ($\overline{\text{OUTPUT}}$)	Synchronous with display output. CMOS level, which is -5.2 V before cursor output address and 0 V after cursor address.
12	Record (OUTPUT)	Low when unit is recording; high otherwise.
9	-5.2 VDC	
8	+5 VDC	
11	Trigger (INPUT)	Logic Level Trigger input must be brought low to enable TTL level.
10	Remote Arm (INPUT)	Line is normally held high and brought low to arm unit.
1, 13	Ground	Power and logic return.

5.2.1 Digital Output Sequence - After Display

Immediately after recording, the 1650-D will enter the display mode, repetitively cycling the memory and producing the X, Y, and Z display signals. In this condition, the Record (pin 12) output signal will be high. The Output Request (pin 2) input will be pulled high.

When a low is input to the Output Request, the Flag (pin 14) will go high, nominally 10 μsec later. Output Request should be held low until the desired memory transfer has been completed. Output Request should then be returned high. When Flag goes high, a Command signal must be input to bring the first sample of the first eight channels out to the output buffers. A second command loads the second eight channels onto the data output pins 18, 19, 16, 17, 22, 23, 24, and 21. All data from this first word to the 500th word are specified to be valid information. The last 12 words are invalid.

The next, and subsequent data words will be presented on the data output lines after each Command (pin 3) input negative transition. For proper data output the interval between Command inputs should be no closer than 8.5 μsec giving asynchronous data word rates 120 K byte per second to DC.

5.2.2 Digital Output Sequence - After Record

If it is desired to output digital data immediately after Record, proceed as follows: hold Output Request (pin 2) low. As soon as Record is complete (Record goes high), Flag (pin 14) will go high, indicating the first data word can be read. When this occurs, proceed with Command Flag operation as described above. When the desired memory length has been transferred, return the Output Request (pin 2) high for further record sweeps.

NOTE: The memory of the 1650-D contains 16 X 512 bits. Only the first through 500th bits of each channel memory are specified to be valid digital output data.

CAUTION: If the ARM IN and/or TRIG IN BNC connectors on the rear panel are enabled, Remote Arm (pin 11) and Trigger (pin 10) must be left floating (high).

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